Claims

1. Method for achieving delay measurement functionality of an integrated circuit comprising the steps of:
   - providing at least one boundary scan cell, each having a storage layer between a scan input port (SI) and a scan output port (SO) constructed to be used within a scan chain for boundary scan testability,
   - analyzing each scan cell to identify a redundant state
   - using this redundant state for creating an additional combinational path (BP) between the scan input port (SI) and a scan output port (SO) of a respective scan cell,
   - implementing each scan cell in the integrated circuit by creating said scan chain.
2. Method of claim 1 wherein the step of providing comprises the providing of the at least one boundary scan cell according to the IEEE Standard 1149.1 or to a standard derived from the IEEE Standard 1149.1.
3. Method of claim 1, wherein the step of creating an additional combinational path comprises the step of implementing a local path (BP) between said respective two scan ports (SI, SO) by bypassing the respective storage layer of a boundary scan cell.
4. Method of claim 1, wherein the combinational path is connected to the scan output port (SO) via a multiplexer (MUX) controlled by the shift signal from a test access port controller.
5. Method of claim 1, comprising the step of connecting the scan input port (SI) of a first scan cell to a test data input port (TDI) for boundary scan testability and the scan output port (SO) of a scan cell forming the end of the scan chain via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan testability.
6. Method of claim 1, comprising the step of connecting the output port

(SO) of a boundary scan cell forming the end of the scan chain to a separate delay chain output port (DCO).

7. Method of claim 1, wherein the combinational path (BP) is defined as false path during synthesizing of the scan chain.

8. A boundary scan cell comprising:

- an input port (PI) and an output port (PO) with a functional layer there between,

- a scan input port (SI) and a scan output port (SO) with a storage layer there between, said storage layer is adapted to be used for achieving boundary scan testability,

- a combinational path (BP) between the scan input port (SI) and the scan output port (SO) bypassing said storage layer.

9. Boundary scan cell of claim 8, wherein the scan cell is based on and conform to the IEEE Standard 1149.1 or a standard derived from the IEEE Standard 1149.1.

10. Boundary scan cell of claim 8, wherein the combinational bypass path (BP) and the storage layer is connected to the scan output port (SO) via a multiplexer (MUX) controlled by the shift signal from a test access port controller.

11. Boundary scan cell of claim 8, wherein the bypass path (BP) comprises at least one additional inverter, library and/or delay element.

12. Integrated circuit comprising
a boundary scan chain having delay measurement functionality.

13. Integrated circuit of claim 12, comprising
at least one boundary scan cell, said scan cell is connected by means of said scan input and output ports (SI, SO) to form a scan chain, wherein the scan input port (SI) of a first scan cell is connected to a test data input port (TDI) and the scan output port (SO) of a scan cell forming the end of the scan chain is connected via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan

testability.

14. Integrated circuit of claim 13, wherein the scan output port (SO) of the boundary scan cell forming the end of the scan chain is connected by means of said test data output path (BSR_TDO) to a separate delay chain output port (DCO).

15. Integrated circuit of claim 14, wherein said test data output path (BSR_TDO) to the delay chain output pot (DCO) is controllable by a test mode signal (TM).

16. Integrated circuit of claim 15, wherein said test mode signal (TM) is similar to a test pin for initializing other testability modes, in particular a RAM-test mode, a PLL test mode and/or a core scan test mode.

17. Electrical device comprising an Integrated circuit of claim 12.

18. Method for performing delay measurement of an integrated circuit comprising a boundary scan chain having delay measurement functionality, including the steps of
- entering a delay measurement mode,
- applying of a test data signal on a test data input (TDI) for boundary scan testability,
- performing the delay measurement at a port (TDO, DCO) connected to the test data output path (BSR_TDO) for scan testability.

19. Method of claim 18, wherein the step of entering comprises the step of entering a test-logic-reset-state.

20. Method of claim 18, comprising the step of
performing the delay measurement at the test data output port (TDO) for boundary scan testability.

21. Method of claim 18, comprising the step of
performing the delay measurement at a separate delay chain output port (DCO).